Please add the following new claims.

176. The method of claim 174 wherein said step of rendering the transistors conductive includes the step of rendering the transistors conductive with a control signal that enables the full voltage representative of a logic level one to be written to the array.

177. A method of controlling the conduction of at least one isolation transistor in a sense amplifier responsive to an array, comprising:

rendering the transistor conductive with a control signal that enables a full Vcc to be conducted by the isolation transistor; and

rendering the transistor nonconductive by removing said control signal.

178. The method of claim 177 wherein said step of rendering the transistor conductive includes the step of rendering the transistor conductive with a control signal that is approximately a Vth higher than Vcc.

179. A method of enabling a write to a memory array of the full voltage representative of a logic level one using a sense amplifier in which the sense amplifiers are located inside the isolation transistors, comprising:

rendering the isolation transistors conductive with a control signal that compensates for the voltage drop across the isolation transistors.

180. The method of claim 179 wherein said rendering step includes the step of rendering the isolation transistors conductive with a control signal that is approximately a Vth higher than the voltage used to represent a logic level one.

181. The method of claim 180 wherein said control signal is approximately Vth plus Vcc.

REMARKS

New claims 176 – 181 are presented for examination. The claims are supported by, for example, FIG. 6C and the text in the paragraph bridging pages 62 and 63. No new matter has been entered.

STATEMENT REQUESTING DELETION OF INVENTOR

As a result of the prosecution of this application, the following individual is no longer an inventor of the subject matter being claimed and should be removed as an inventor:

Scot J. Derner

Please allow the instant application to proceed in the names of the remaining inventors (Keeth and Bunker) in accordance with 37 CFR 1.63 (d).

It is respectfully requested that the instant application, covering claims 174 – 181 receive an early office action on the merits.

Respectfully submitted

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Dated: 7 November 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:** Not yet assigned
Serial No.:	09/934,795	)	
		)	**Art Unit:** 2816
Filed:	22 August 2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

COMPLETE CLEAN SET OF PENDING CLAIMS

174. (Amended) A method of controlling the conduction of a pair of isolation transistors in a sense amplifier responsive to an array, comprising:

rendering the pair of transistors conductive with a control signal that is a boosted version of the voltage used by the array; and

rendering the pair of transistors nonconductive by removing said control signal.

175. (Amended) The method of claim 174 wherein said step of rendering the pair of transistors conductive includes the step of rendering the transistors conductive with a control signal that is approximately a Vth higher than the voltage used by the array.

176. The method of claim 174 wherein said step of rendering the transistors conductive includes the step of rendering the transistors conductive with a control signal that enables the full voltage representative of a logic level one to be written to the array.

177. A method of controlling the conduction of at least one isolation transistor in a sense amplifier responsive to an array, comprising:

rendering the transistor conductive with a control signal that enables a full Vcc to be conducted by the isolation transistor; and

rendering the transistor nonconductive by removing said control signal.

178. The method of claim 177 wherein said step of rendering the transistor conductive includes the step of rendering the transistor conductive with a control signal that is approximately a Vth higher than Vcc.

179. A method of enabling a write to a memory array of the full voltage representative of a logic level one using a sense amplifier in which the sense amplifiers are located inside the isolation transistors, comprising:

rendering the isolation transistors conductive with a control signal that compensates for the voltage drop across the isolation transistors.

180. The method of claim 179 wherein said rendering step includes the step of rendering the isolation transistors conductive with a control signal that is approximately a Vth higher than the voltage used to represent a logic level one.

181. The method of claim 180 wherein said control signal is approximately Vth plus Vcc.